FRIL ADAPTOR SPECIFICATION

2/24/77

MURF

CONFIDENTIAL PROPRIETARY INFORMATION

FRIL ADAPTOR

LIST OF ILLUSTRATIONS

1.0 General Description

The Datapoint FRIL (Fast Resource Intercom Link) Adaptor is a special purpose communications adaptor designed to provide high speed communications between a number of Datapoint processors (throughout this specification the term 'processor' denotes any Datapoint processor with an input/output bus compatible with the Datapoint 2200). Data is carried over coaxial cable at 2,500,000 bits per second in a unique Datapoint format. The system incorporates a self-polling feature that eliminates the need for a master station in the system. Data is moved over the coax in variable length (1 to 253 bytes) packets. Each Adaptor has a unique identificatiion number and Packets may be sent to one specific Adaptor or broadcast to all Adaptors in the system. Adaptors receive only those packets addressed to them or broadcasted to all Adaptors (reception of BROADCASTS may be inhibited under processor control). Packets are interleaved so that the system can simultaneously support a number of independent communications paths without the processors realizing that they do not have exclusive use of the system.

2.0 System Requirements

2.1 System Components

The FRIL Adaptor is a self-powered unit which may be mounted on the back of any Datapoint console table or on any flat surface. Interface to the processor is via a Universal I/O Cable.

If there are more than two FRIL Adaptors in the system, one or more FRIL HUBS will be required.

2.2 System Configuration (see FIG 2-1)

If there are only two FRIL Adaptors in the system they may be directly connected together with a length of coax. If there are three or more FRIL Adaptors each one must be connected, with a length of coax, to a port on either a FRIL Hub Card, installed in a Port Expander Chassis, or a FRIL LINE SPLITTER. Large systems may require several interconnected Hub Cards and LINE SPLITTERS.

A FRIL LINE SPLITTER may be used to interconnect up to four FRIL Adaptors and/or FRIL Hub Card ports, with the restriction that the sum of the longest two lengths of coax connected to the LINE SPLITTER may not exceed 200 feet.

A FRIL Hub Card, installed in a Port Expander Chassis, may be used to interconnect up to 8 FRIL Adaptors, or a combination of up to 8 ports on either LINE SPLITTERS or Hub Cards installed in other Port Expander Chassis. Two Hub Cards may be installed in a single Port Expander Chassis to provide 16 ports. Up to 2000 feet of coax may be used between an Hub Card port and a FRIL Adaptor or a port on another Hub Card. Up to 255 FRIL Adaptors may be installed in a single system with the restriction that there be no more than twenty Hub Card ports in any single path. All coax must be either RG-62A (solid center conductor) or RG-62B (stranded center conductor) terminated with male BNC connectors.

3.0 Technical Description

3.1 FRIL Adaptor Description

The FRIL Adaptor consists of six sections; BUFFER, STATUS WORD, CONTROLLER, TRANSMITTER, RECEIVER, AND LINE INTERFACE. The processor can transfer data to and from the BUFFER and test and reset bits in the STATUS WORD. The CONTROLLER can transfer data from the BUFFER to the TRANSMITTER or from the RECEIVER to the BUFFER and test and set bits in the STATUS WORD. The LINE INTERFACE interfaces the TRANSMITTER and RECEIVER to the coaxial line.

The adaptor contains a 1024 byte memory which is used as a random access speed buffer between the processor and the adaptor's transmitter and receiver. The buffer memory is divided into 4 pages of 256 bytes each.

There are three page registers; one each for the processor, the TRANSMITTER, and the RECEIVER . All INPUT, PIN, and MIN instructions when the adaptor is in DATA mode and all EX WRITE and MOUT instructions act on the buffer page selected by the processor page regiister. The TRANSMITTER reads data from the buffer page selected by the transmitter page register. The RECEIVER writes data into the buffer page selected by the receiver page register. The page registers are independent and remain set until changed by EX COM1 commands.

Data transfers to or from the processor may be made at any time, whether or not the transmitter or receiver is busy and indepedent of any status bits. These transfers may be made at the full MIN/MOUT rate of the Datapoint 5500 processor. Care should be taken that transfers not be made from the processor to the page accessed by the transmitter when the transmitter is not available or to the processor from the page accessed by the receiver until the receiver is inhibited. Unless a specific address is provided, the buffer memory will automatically address sequentially within each page.

3.2 Line Protocol (see FIG 3-1)

The line idles in a spacing (logic 0) condition. A transmission starts with an ALERT BURST consisting of six unit intervals of mark (logic 1). Eight bit characters are then sent with each character preceeded by two unit intervals of mark and one unit interval of space. Five types of transmission are sent:

INVITATIONS TO TRANSMIT

An ALERT BURST followed by three characters; an EOT (End Of Transmission) and two (repeated) DID

(Destination IDentification) characters. Used to pass control of the line from one adaptor to another.

FREE BUFFER ENQUIRIES
An ALERT BURST followed by three characters; an ENQ (ENQuiry) and two (repeated) DID (Destination IDentification) characters. Used to ask an adaptor if it is able to accept a packet.

PACKETS
An ALERT BURST followed by from 8 to 260 characters; a SOH (Start Of Header), a SID (Source IDentification), two (repeated) DID's (Destination IDentification), a COUNT, from 1 to 253 data characters, and two CRC (Cyclic Redundancy Check) characters. Used to move data between adaptors.

ACKNOWLEDGEMENTS
An ALERT BURST followed by one character; an ACK (ACKnowledgement). Used to acknowledge PACKETS and as an affirmative response to FREE BUFFER ENQUIRES.

NEGATIVE ACKNOWLEDGEMENTS
An ALERT BURST followed by one character; a NAK (Negative AcKnowledgement). Used as a negative response to FREE BUFFER ENQUIREs.

The receiver validates all incoming transmissions by checking for:

At least one mark and exactly one space preceeding each character;

An EOT, ENQ, SOH, ACK, or NAK following the ALERT BURST;

Proper CRC (packets only);

Proper number of characters (3, 8 to 260, or 1);

At least nine spaces following the last character.

3.3 Link Control (see FIG 3-2)

Each FRIL Adaptor in a system has a unique ID (IDentification) from 1 to 0377 selected by jumpers in the adaptor. (ID 0 may not be assigned to any FRIL Adaptor

since destination 0 is used to indicate a BROADCAST to all adaptors!). System operation is based on an INVITATION TO TRANSMIT being passed around the system with each adaptor passing it to NID (Next ID), the adaptor with the next higher ID in the system. When an adaptor receives an INVITATION TO TRANSMIT containing its ID it assumes control of the line. Which adaptors are in the system is determined during SYSTEM RECONFIGURATION.

When an adaptor is first turned on, or has not received an INVITATION TO TRANSMIT for approximately 500 ms., it causes a SYSTEM RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 510 times. The purpose of this burst is to terminate all activity on the line. It is longer than any other type of transmission and will therefore interfere with the next INVITATION TO TRANSMIT and keep any adaptor from seeing it and assuming control of the line. It also provides line activity so that the adaptor sending the INVITATION TO TRANSMIT releases control of the line. Thus the adaptor that had control releases it and no other adaptor picks it up. When any adaptor sees idle line for 78.2 us. it knows the system is being reconfigured and initializes its NID to its own ID. It then starts a time-out equal to 146 us. times 255 minus its own ID. If this time-out expires with no line activity the adaptor starts sending INVITATIONs TO TRANSMIT. (Note that this time-out will expire only in the adaptor with the highest ID in the system.)

After sending an INVITATION TO TRANSMIT the adaptor waits for activity on the line (the adaptor receiving the invitation sending a FREE BUFFER ENQUIRY, PACKET, or INVITATION TO TRANSMIT or any adaptor sending a RECONFIGURATION BURST). If there is no activity for 74.7 us. the adaptor increments NID and tries again. If it hears any activity before the time-out expires it releases control of the line. During SYSTEM RECONFIGURATION INVITATIONs TO TRANSMIT will be sent to all 256 possible ID's. Each adaptor, however, will have saved NID, the ID of the adaptor that assumed control from it. From then until the next SYSTEM RECONFIGURATION (which will occur only when a new adaptor is powered up or when an adaptor gets dropped from the system due to line errors causing it to miss an INVITATION TO TRANSMIT), control is passed directly from adaptor to adaptor with no wasted INVITATIONs TO TRANSMIT sent to ID's not in the system.

The time required to do a SYSTEM RECONFIGURATION depends on the number of adaptors in the system and the propagation delays between them, but will be in the range of 25 to 65 ms.

3.4 Commands

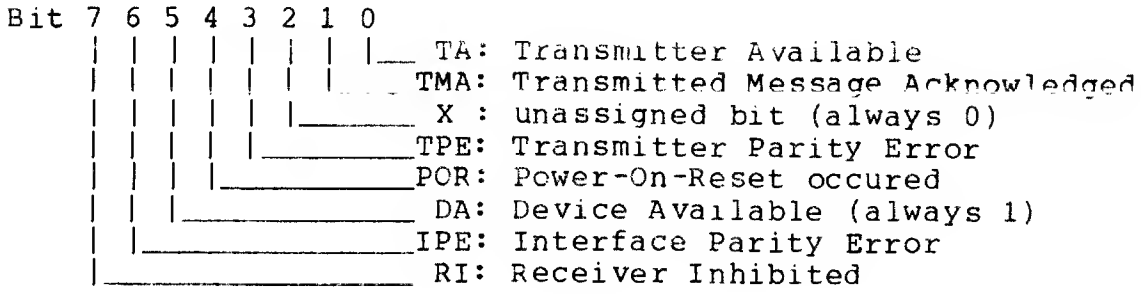
All communications between the FRIL Adaptor and the processor is via the input/output bus using the External Command, INPUT, PIN, MIN, and MOUT instructions. (See processor reference manual.)

EX ADDRESS

Sets ADDRESSED and STATUS modes in the adaptor if proper address is present on processor outbus. ADDRESSED mode remains set until another I/O device is addressed with another EX ADDRESS. EX ADDRESS is the only command recognized by the adaptor when ADDRESSED mode is not set.

EX STATUS

Sets STATUS mode in the adaptor so that the status word will be transferred to the processor when an INPUT instruction is executed. See section on EX COM1 and section 3.5 for use of the status word. The status word format is as follows:



EX DATA

Sets DATA mode in adaptor so that data from buffer will be transfered to processor when an INPUT instruction is executed.

INPUT

Transfers the status word or data to the processor. Data transfer is from the current processor page and address in buffer memory. Address wrap-around, within the selected page, occurs when byte 0377 is transfered. The FRIL Adaptor also supports the PIN and MIN instructions implemented in certain processors in both STATUS and DATA modes.

EX WRITE

Transfers a word from the processor to the current processor page and address in the adaptor buffer. At completion of transfer the address is incremented. Address wrap-around, within the selected page, occurs when byte 0377 is transferred. The FRIL Adaptor also supports the MOUT instruction implemented in certain processors.

EX COM1

EX COM1 is a general adaptor command whose purpose is defined by the contents of the processor output bus as follows:

00 000 000 Clear IPE: clears Interface Parity Error status bit.

00 000 001 Disable TRANSMITTER: causes TRANSMITTER to cancel any previous uncompleted command to transmit. TA (Transmitter Available) will come true within 400 ms. to indicate acceptance of this command. (Note that TA comes true in response to this command the next time the adaptor receives an INVITATION TO TRANSMIT and that its failure to do so within 400 ms. would be an indication that there are no other operating FRIL Adaptors in the system!)

00 000 010 Disable RECEIVER: causes RECEIVER to cancel any previous uncompleted command to receive. RI (Receiver Inhibited) will come true within 400 ms. to indicate acceptance of this command. (Note that RI comes true in response to this command the next time the adaptor receives an INVITATION TO TRANSMIT and that its failure to do so within 400 ms. would be an indication that there are no other operating FRIL Adaptors in the system!)

00 0nn 011 Select processor page: Sets processor buffer page to nn. All INPUT, PIN, and MIN instructions when the adaptor is in DATA mode and all EX WRITE and MOUT instructions act on the buffer page selected by this command.

00 0nn 100 Enable transmit from page nn: Sets transmitter buffer page to nn, clears TA (Transmitter Available), TMA (Transmitted Message Acknowledged), and TPE (Transmitter Parity Error) status bits and causes adaptor to start a transmit sequence. Status bit 0 (TA) returns

true upon completion of the transmit sequence. Status bit 1 (TMA) will have been set by this time if the adaptor has received an acknowledgement from the destination adaptor. (Note that this is strictly a hardware level acknowledgement which is sent by the receiving adaptor before its host processor is even aware that a packet has been received. Note also the acknowledgement may get lost due to line errors so that TMA not being set is not a guarantee that the packet was not received.) Status bit 3 (TPE) will have been set by this time if the transmitter read a byte with bad parity from the buffer while sending the packet, in which case the transmission was aborted without sending a CRC, insuring that the destination adaptor did not receive a packet containing errors. This command should not be executed unless TA (status bit 0) is true!

00 0nn 101 Enable receive to page nn: Sets receiver buffer page to nn, clears RI (Receiver Inhibited) status bit, and allows the adaptor to receive. Status bit 7 (RI) will return true only when a packet addressed to the adaptor, or a BROADCAST (if reception of BROADCASTs has been enabled), has been received and, except in the case of BROADCASTs, acknowledged. This command should not be executed unless RI (status bit 7) is true!

00 000 110 Clear POR: Clears Power-On-Reset status bit. If either the FRIL Adaptor or its host processor loses its operating power this status bit is set upon resumption of power. The adaptor sets the TA and RI status bits after a Power-On-Reset, but the state of the TMA, TPE, and IPE status bits and the contents of the buffer are indeterminate.

EX COM4

Sets buffer address to the contents of the processor output bus and sets DATA mode in the adaptor. All three page registers remain unchanged. The next EX WRITE or INPUT instruction executed will access the location in the buffer memory specified by this address and the processor page register.

3.5 Programming

To transmit a message the processor selects a buffer for its use (EX COM1 with A=0N3 where N is 0, 1, 2, or 3), and writes into the buffer (EX COM4 and EX WRITE) in the following format:

ADDR	0000	XXX	- Unused
ADDR	0001	DID	- Destination IDentifier (000 for BROADCAST)
ADDR	0002	COUNT	- 2's complement of DATA length
ADDRs	COUNT-0377	DATA	- Message to be sent

The processor then waits for TA (status bit 0) to be true and gives the transmit command (EX COM1 with A=0N1). At the completion of its transmit sequence the adaptor conditionally sets TMA (status bit 1) and TPE (status bit 3) and then sets TA.

If the DID is non-zero (the PACKET is not a BROADCAST) the FRIL Adaptor will wait for a free buffer (RI false) at the destination (without locking out other users) before sending the packet. Note that if the host processor at the destination is not servicing its FRIL Adaptor the adaptor at the source will never find a free buffer and never set TA. There must, therfore, be a software time-out on TA. When this timer times out the processor should disable the TRANSMITTER (EX COM1 with A=001) to force the adaptor to abandon the transmission. Note that if the disable TRANSMITTER command does not cause TA to return true within 400 ms. it is an indication that there are no other FRIL Adaptors in the system.

To enable the receiver the processor assigns a buffer for its own use (EX COM1 with A=0N3), sets the buffer address to 001 (EX COM4 with A=001), writes a 000 to enable reception of BROADCASTS or any non-zero byte to inhibit reception of BROADCASTS, waits for RI (status bit 7) to be true, and gives the receive command (EX COM1 with A=0N2). When a packet addressed to the local adaptor or sent as a BROADCAST (if reception of BROADCASTs was enabled) is completely and correctly received the adaptor sets RI. The processor selects the buffer used by the receiver for its own use (EX COM1 with A=0N3) and reads the buffer (EX COM4, and IN). The buffer contents are as follows:

ADDR	0000	SID	- Source IDentifier
ADDR	0001	DID	- Local ID or 000 (BROADCAST)
ADDR	0002	COUNT	- 2's complement of DATA length
ADDRs	COUNT-0377	DATA	- Received message

Note that the usual range of the COUNT is 0377 (1 DATA byte) to 003 (253 DATA bytes). The COUNT may also be set to

002 or 001 in which case 253 DATA bytes will be sent (buffer locations 0003 to 0377), just as if the COUNT were 3. Thus the COUNT may be used to carry 'extra' information on full length packets.

3.6 Data Exchange (see FIG. 4)

When an adaptor receives an INVITATION TO TRANSMIT it checks to see if it has a packet to send, i.e. if TA (Transmitter Available) is false. If not it sends an INVITATION TO TRANSMIT to NID. Otherwise it tests byte 001 in the transmit buffer, the DID (Destination IDentifier). If this byte is 000 the packet is a BROADCAST and the adaptor sends the packet. Otherwise it sends a FREE BUFFER ENQUIRY to the DID adaptor and waits up to 75.1 us. for a response. If the response to the FREE BUFFER ENQUIRY is an ACK it sends the packet. If after sending the COUNT it finds that the COUNT has been set to 000 it truncates the rest of the packet (insuring that no Adaptor will receive it), sets TA, and sends an INVITATION TO TRANSMIT to NID. If the response to the FREE BUFFER ENQUIRY is a NAK it sends an INVITATION TO TRANSMIT to NID and will send another FREE BUFFER ENQUIRY the next time it receives an INVITATION TO TRANSMIT. If the adaptor times-out waiting for a response to the FREE BUFFER ENQUIRY it sets TA and sends an INVITATION TO TRANSMIT to NID.

After sending a packet the adaptor waits up to 75.1 us. for a response. If it receives an ACK it sets TMA and then TA and sends an INVITATION TO TRANSMIT to NID. If it times out waiting for an ACK (packets are never NAK'ed) it just sets TA and sends an INVITATION TO TRANSMIT to NID.

When an adaptor receives a FREE BUFFER ENQUIRY it tests RI. If RI is true it sends a NAK. Otherwise it sends an ACK.

When an adaptor receives an SOH (indicating the start of a PACKET) it writes the SID into the receive buffer and then checks the first DID. If this byte is 000 (indicating a BROADCAST) the Adaptor tests byte 001 in the receive buffer for a 000 (reception of BROADCASTs enabled). If reception of BROADCASTs is enabled, or if the first DID is the adaptor's own ID, the adaptor writes the second DID, and the rest of the PACKET into the receive buffer. Otherwise it ignores the rest of the PACKET. If after being written into the receive buffer the PACKET fails either the CRC or length validation phases, the adaptor ignores it. Otherwise it tests byte 001 in the receive buffer, the DID. If this

byte is 000 the packet is a BROADCAST and the adaptor simply sets RI. If this byte is the adaptor's own ID the adaptor sends an ACK before setting RI. If the DID is neither 000 nor the adaptors own ID the adaptor ignores the packet.

4.0 PHYSICAL DESCRIPTION

Figure 4-1 shows the dimensions of the FRIL Adaptor, its controls and interface connectors.

5.0 ENVIRONMENTAL REQUIREMENTS

0°C to 50°C (32°F to 122°F) operating ambient

10% to 95% relative humidity (non-condensing)

6.0 INTERFACE DESCRIPTION

6.1 INPUT/OUTPUT REQUIREMENTS

The FRIL Adaptor interfaces with the I/O bus through J1. J2 has the same pin assignments as J1 so that additional external device controllers and adaptors may be connected to the processor parallel I/O bus by daisy-chaining the devices with Universal I/O cables.

The FRIL Adaptor interfaces to the other Adaptors in the system through BNC connector J3.

6.2 POWER REQUIREMENTS

The FRIL Adaptor contains its own power supply which may be strapped for any common line voltage as described in section 7.1.

An ON/OFF switch and an INTERLOCK switch are provided. When the ON/OFF switch is in the ON posiition and the INTERLOCK switch in the ENABLE position the FRIL Adaptor is "slaved" to the processor and is turned on and off automatically when the processor is turned on and off. When the INTERLOCK switch is in the DEFEAT position the FRIL Adaptor is turned on and off by the ON/OFF switch without regard for the state of the processor.

7.0 FIELD SELECTABLE OPTIONS

7.1 Power

Field alterable straps are provided to allow operation from 100, 115, 127, 220, 240, or 260 VAC +/- 10%, 47 to 63 Hz.

7.2 Address

The FRIL Adaptor device address may be set to any of the available addresses in the field by means of jumpers. The FRIL Adaptor is wired for address 0234 at the factory. Addresses 0232, 0231, 0254, 0252, and 0251 are reserved for the second, third, fourth, fifth, and sixth FRIL Adaptors hosted by the same processor.

7.3 ID

The FRIL Adaptor's unique ID may be set to any address from 1 to 0377 in the field by means of switches. NO TWO ADAPTORS IN THE SAME SYSTEM MAY HAVE THE SAME ID, NOR MAY ANY ADAPTOR HAVE IT'S ID=000!

7.4 Processor Selection

A jumper is provided to inhibit I/O parity checking for use with processors which do not use parity on the I/O bus.

8.0 SHIPPING LIST

The following items are shipped with each FRIL Adaptor:

Quanity	Item
1	FRIL Adaptor Specification
1	FRIL Adaptor Maintainance Bulletin
1	I/O Cable

NOTE: The following items should be ordered with each FRIL Adaptor:

Quanity	Item
2	Male BNC connectors
1	coax cable (specify length)

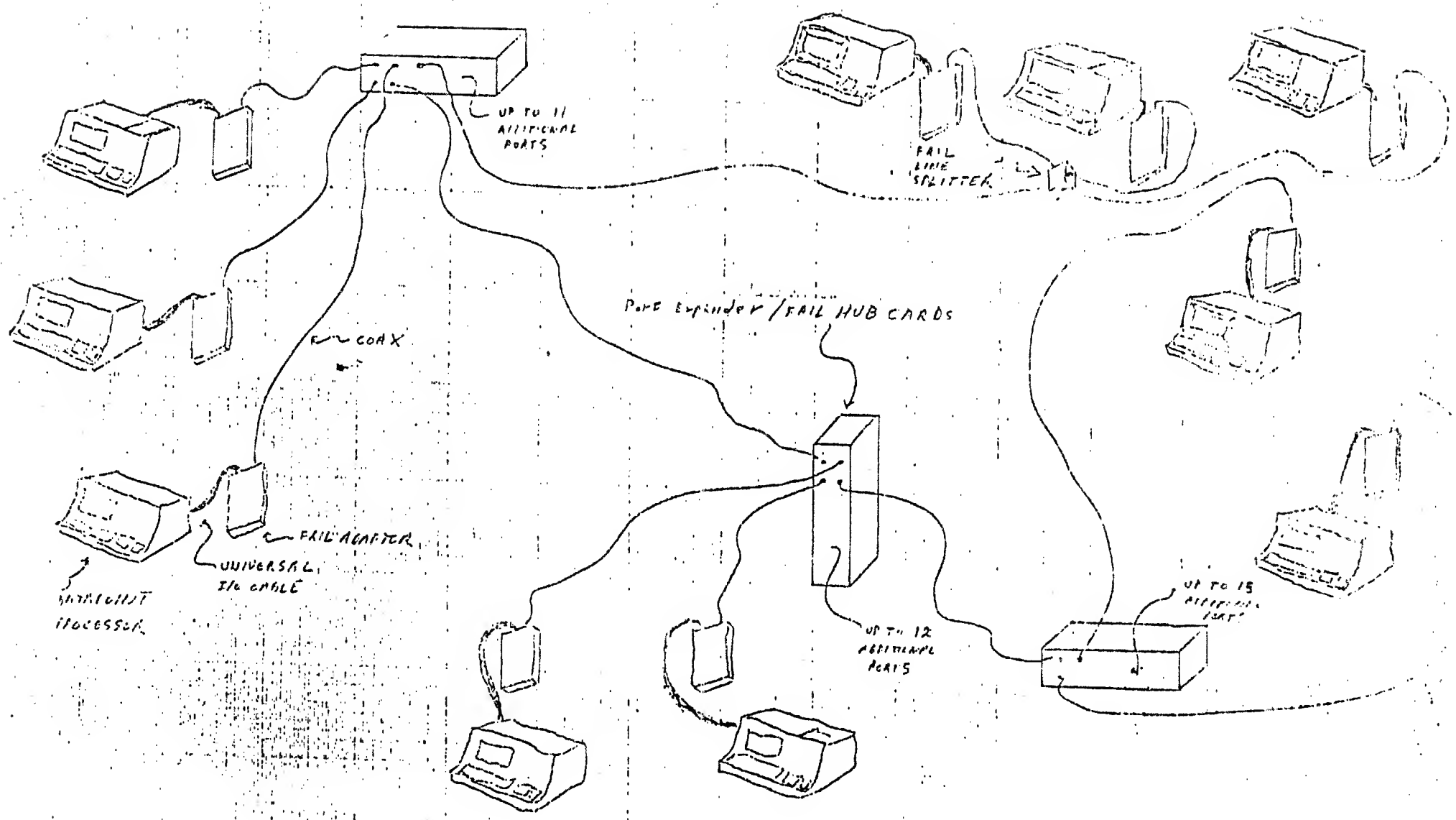
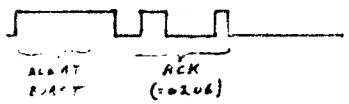

UP TO 11 ADDITIONAL PORTS
FAIL LINE SPLITTER
PORT EXPANDER / FAIL HUB CARDS
COAX
FAIL ADAPTER
UNIVERSAL I/O CABLE
UP TO 12 ADDITIONAL PORTS
UP TO 15 ADDITIONAL PORTS

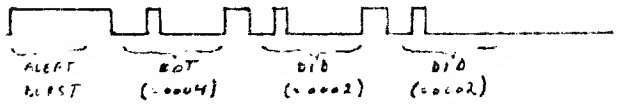
FIG. 2-1

TYPICAL TRANSMISSION AS SEEN AT TRANSMITTER OR RECEIVER

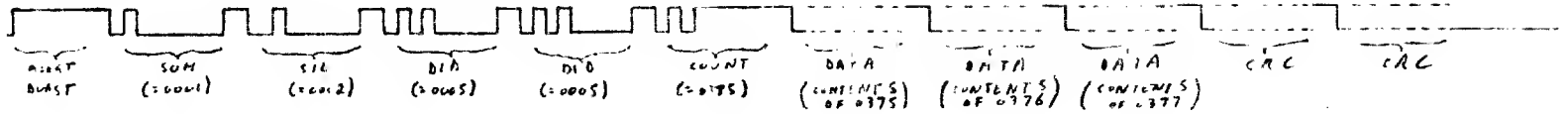
ACKNOWLEDGEMENT



INVITATION TO TRANSMIT (to FAIL #2)



PACKET (from FAIL #2 to FAIL #5, COUNT=0375)



TYPICAL TRANSMISSION AS SEEN AT COAXIAL LINE

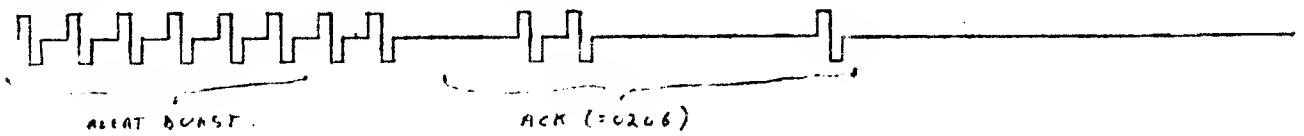
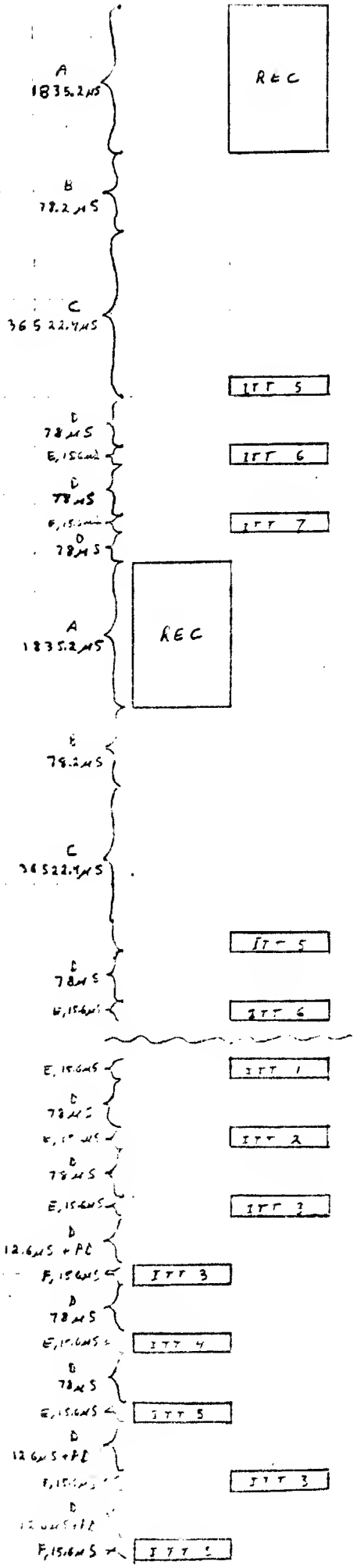


FIG 3-1 TRANSMISSION FORMAT



LEGEND:

REC RECONFIGURATION BURST

ITT n; INVITATION TO TRANSMIT to Adapter # n

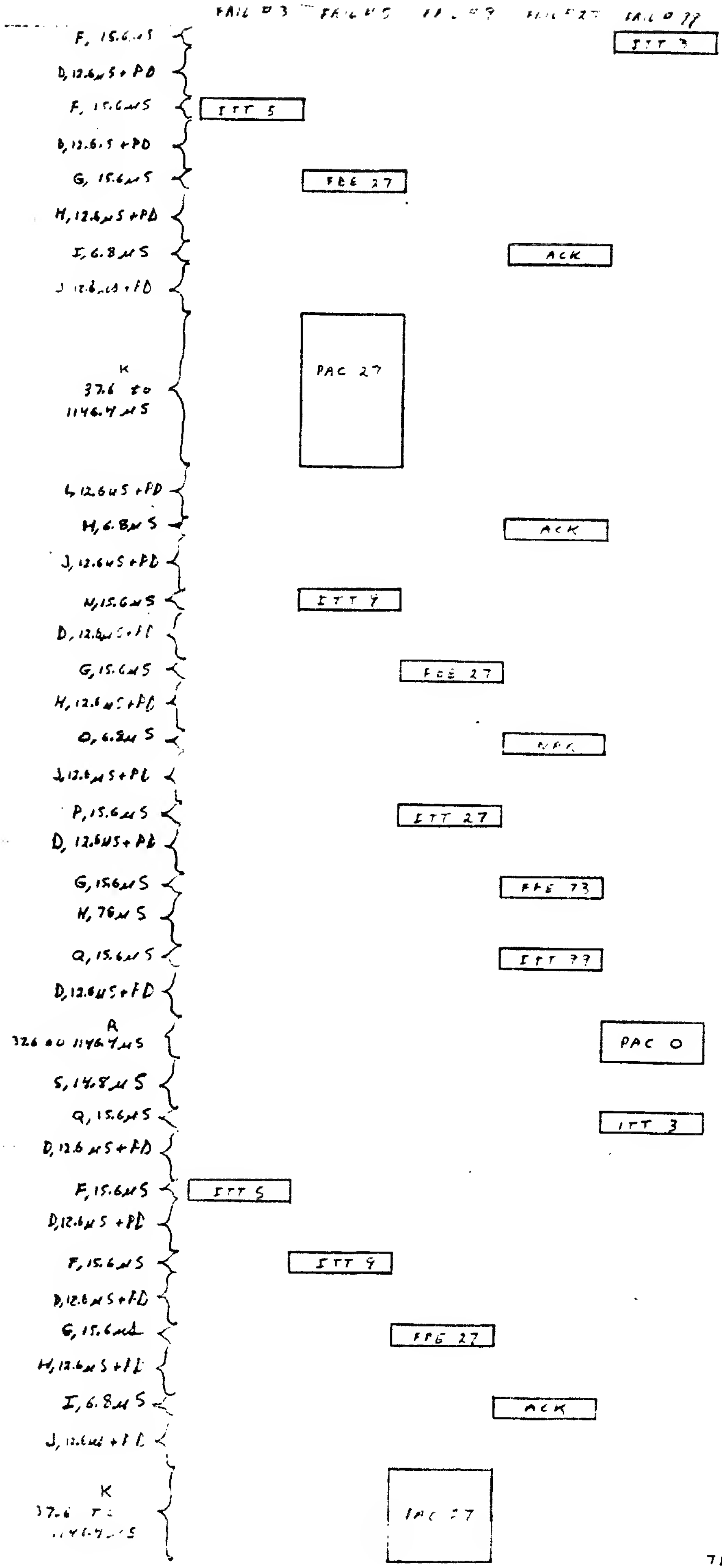
A thru F; Event references. See Notes for FIG. 3 & FIG. 4

PD : Propagation Delay, varies with length of coax and observers physical position in system.

FIG 3-2

TYPICAL SYSTEM RECONFIGURATION

(Adapt # 3 powered up second in system. Adapter # 5)



LEGEND:

ITT n ; INVITATION TO TRANSMIT TO adaptor # n

FBE n ; FREE BUFFER ENQUIRY to adaptor # n

ACK ; ACKNOWLEDGEMENT

PAC n ; PACKET to adaptor # n

NAK ; NEGATIVE ACKNOWLEDGEMENT

F thru R ; Event references. See "NOTES for FIG. 4"

PD ; Propagation Delay varies with length of cable and observed physical position in system

FIG 3-3

TYPICAL DATA EXCHANGES

FIG 3-4 NOTES for FIG 3-2 and FIG 3-3

EVENT	TIME (us)	DESCRIPTION
A	1835.2	An adaptor powers up, sends a RECONFIGURATION BURST, and sets NID=MYID. The adaptor in control of the system (if there is one) relinquishes control.
B	78.2 (-0,+5.25)	All adaptors recognize idle line condition, set NID=MYID, and start a time-out equal to 146 us. times 255-MYID.
C	146(255-HIID)+22.4	Adaptor with highest numbered ID (HIID) times out, assumes control of the system, and sends an INVITATION TO TRANSMIT to NID (=MYID at this time due to event A or B). All other adaptors recognize that an adaptor with a higher ID number is in the system, terminate the time-out started in EVENT B, and wait for an INVITATION TO TRANSMIT.
D	12.6 to 78	Adaptor in control of system waits for line activity in response to its INVITATION TO TRANSMIT.
E	15.6	Adaptor in control of system times out after 74.7 us., increments NID, and sends an INVITATION TO TRANSMIT to its new NID.
F	15.6	Control of system is passed. Adaptor now in control has no packet to send and therefore sends an INVIATION TO TRANSMIT to NID.
G	15.6	Control of system is passed. Adaptor now in control has a non-BROADCAST packet to send and therefore sends a FREE BUFFER ENQUIRY to DID.
H	12.6 to 78	Adaptor in control of system waits for an ACK or NAK response to his FREE BUFFER ENQUIRY.

FIG 3-4 NOTES for FIG 3-2 and FIG 3-3 (continued)

EVENT	TIME (us)	DESCRIPTION
I	6.8	Adaptor receiving FREE BUFFER ENQUIRY has RI reset and therefore responds by sending an ACKNOWLEDGEMENT.
J	12.6+PD	The response propagates back to the adaptor in control of system.
K	37.6 to 1146.4	Adaptor in control of system sees ACKNOWLEDGEMENT response to his FREE BUFFER ENQUIRY and sends a PACKET.
L	12.6 to 78	Adaptor in control of system waits for ACK response to his PACKET.
M	6.8	Adaptor receiving PACKET addressed to him sends ACKNOWLEDGEMENT and sets RI.
N	15.6	Adaptor in control of system sees ACKNOWLEDGEMENT response to his PACKET, sets TMA, set TA, and sends an INVITATION TO TRANSMIT to NID.
O	6.8	Adaptor receiving FREE BUFFER ENQUIRY has RI set and therefore responds by sending a NEGATIVE ACKNOWLEDGEMENT.
P	15.6	Adaptor in control of system sees NEGATIVE ACKNOWLEDGEMENT response to his FREE BUFFER ENQUIRY and sends an INVITATION TO TRANSMIT to NID.
Q	15.6	Adaptor in control of system times-out after 75.1 us., sets TA, and sends an INVITATION TO TRANSMIT to NID.
R	37.6 to 1146.4	Control of system is passed. Adaptor now in control has a BROADCAST packet to send and does so.

FIG 3-4 NOTES for FIG 3-2 and FIG 3-3 (continued)

EVENT	TIME (us)	DESCRIPTION
S	14.8	Adaptor in control of system waits 14.8 us. after sending BROADCAST packet and sends an INVITATION TO TRANSMIT to NID.